REMARKS

In paragraph 4, page 2 of the Office Action mailed January 7, 2003, the Examiner stated that the "proposed drawing correction/and or the proposed substitute sheets of drawings filed on 19 May 1998 in the applicant's provisional U.S. Patent Application No. 60/086,153 have been disapproved because they introduce new matter into the drawings." The Applicant respectfully reminds the Examiner that no new matter is introduced by an original filing of a provisional application and therefore the Examiner's disapproval of the drawings based upon 37 CFR 1.121(a)(6) is unfounded.

At page 3, second paragraph of the Office Action, the Examiner states that incorporating by reference "Assignment Decision Diagram for High-Level Synthesis" by Viraphol Chaiyakul and Daniel D. Gajski, Technical Report #92-102, December 12, 1992 was improper due to the belief of the Examiner that the cited reference was essential matter. The Applicant, however, disagrees with the Examiner since the reference is "subject matter referred to for purposes of indicating the background of the invention or illustrating the state of the art." (see MPEP 608.01(p)(A)) The reference was cited as a convenience for the reader and is therefore non-essential subject matter that can be incorporated by reference.

Also at page 3, fourth paragraph of the Office Action, the Examiner states that the "amendment to the specification, as compared to the priority document (provisional U.S. Patent Application No. 60/086,153 filed 24 March 1999[1]) is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure." The Applicant again respectfully reminds the Examiner that the non-provisional application 09/275,527 was originally filed on 24 March 1999 and therefore no amendment to the specification was made. Therefore, no new matter was added by amendment as stated by the Examiner and cancellation of "new matter" as requested by the Examiner is also unfounded. Additionally, a rejection under 132 for differences between a provisional and a non-provisional is improper since the provisional, by definition, only provides priority for claims that it supports.

All claims were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor, at the time the application was filed, had possession of the claimed invention. The Applicant believes that the provisional application properly provides support for all claims in non-provisional application.

At page 4, the Examiner stated that it is his belief that the term "non-atomic refers to Hardware Description Language (HDL) source code that is used in a behavioral circuit simulation." The Applicant respectfully disagrees since the term "atomic" is an adjective that is clearly defined at page 3 second paragraph of the specification, "By atomic, it is meant that the process block can not be analyzed beyond the inputs (stimuli) provided and the corresponding outputs generated" thereby restricting the ability of the circuit designer to adequately characterize, debug, and/or analyze the complex digital circuit being simulated. Therefore, the term non-atomic does not refer to source code itself but rather is an adjective that refers to a **process block that can be analyzed** beyond the inputs and corresponding outputs generated.

Claims 1, 2, and 6 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,296,467 issued to Chang in view of "Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski (hereinafter Chaiykul) and further in view of U.S. Patent 5,920,711 issued to Seawrite et al. It should be noted that the Chang reference was filed 30 September 1999 taking priority from provisional application 60/102,566 filed 30 September 1998. Accordingly, since the Applicant believes that the instant application properly takes priority from provisional Application No. 60/086,153 filed on 19 May 1998, the Chang reference is therefore not prior art and cannot be used to render the rejected claims unpatentable. However, even in the event that the Chang reference is prior art, the Chang reference taken with the secondary references do not render claims 1, 2, and 6 as being unpatentable for at least the following reasons.

Chang describes a block based design methodology for designing a circuit system that includes selecting a plurality of pre-designed circuit blocks. These circuit blocks are strictly atomic in nature in that the block cannot be analyzed beyond the input stimuli and the corresponding outputs generated. At no point does Chang even remotely suggest determining a state within a particular circuit block since the system of Chang only involves determining output behavior based upon provided input stimuli. For example, at column 12, lines 56 – 60, "It can be used to examine a subset of chip behaviors or block interactions which need to be studied in detail to guarantee sufficiency or to guarantee that resolution provided by any existing simulation model for the block is sufficient." In this way, **Chang only references behavior at the block level and does not comprehend a state or behavior *within* the block** therefore demonstrating the atomic nature of Chang. The *Chaiyakul* reference merely provides a general description of

[1] The Examiner appears to be citing the filing date of the non-provisional application of 24 March 1999 and not the filing date of the provisional application of 19 May 1998.

the ADD and does not teach or reasonably suggest annotating the ADDs described with control nodes that provide a window into the state of the ADD at a particular point associated with the control node. The Examiner attempts to overcome this acknowledged (by the Examiner) deficiency by citing *Seawrite* which merely provides a breakpoint and does not teach or reasonably suggest the use of a control node to provide access to or control of a state within the ADD as does the invention described in more detail below.

The invention as recited in claim 1 requires,

> "converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used by a simulator to simulate behavior of the process block; and
>
> annotating the ADD representation of the process block with one or more control nodes wherein when a particular control node is encountered, **the state within the process block associated with the control node can be directly observed** thereby substantially eliminating an atomic nature of the process block so as to provide a non-atomic analysis of the behavioral model." (emphasis added)

Therefore, in contrast to the cited references, the invention as recited in claim 1 describes a non-atomic "annotated assignment decision diagram" approach to logic simulation by use of control nodes annotating an associated assignment decision diagram. By annotation it is meant that selected portions of a particular ADD are associated with any of a number of control nodes which can be used to stop, start, view, etc. the state of the ADD at any selected point within the ADD. Therefore, the control nodes afford the ability to observe the states **within** a particular process block and not just the global (i.e., atomic) state of a process block as required by the cited references. By affording the ability to observe a state within a process block, the logic simulation provided by the invention is more easily debugged and provides a more detailed description of the process being simulated than is possible by any approach contemplated by the references taken singly or in any combination.

Accordingly, the Applicant believes that claim 1 is neither anticipated or rendered obvious by any of the cited references taken singly or in any combination and is therefore allowable.

Independent claim 7 has been amended to recite substantially the same limitations of claim 1 albeit as a behavioral model, provided on a machine readable medium and is therefore allowable for at least the reasons stated for independent claim 1.

The Examiner rejected a number of dependent claims under the above cited references further in view of U.S. Patent 6.421,808 issued to McGeer which adds nothing to the already cited references that renders any of the rejected dependent claims as unpatentable.

The Examiner rejected claims 11 – 26 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,937,190 issued to Gregory (hereinafter referred to as Gregory 1) in view of U.S. Patent 5,870,608 issued to Gregory further in view of Chaiykul and further in view of McGeer. Gregory 1 teaches architecture and methods for hardware description language source level analysis and does not teach or even remotely suggest use of control nodes to provide a non atomic view of a state within a particular process block.

Independent claim 11 recites in part,

> "(f) annotating the assignment decision diagram (ADD) with a plurality of selected control nodes that are responsible for maintaining control flow through the simulator, wherein when a particular control node is encountered, a state within the process block associated with the control node can be directly observed thereby substantially eliminating an atomic nature of the process block"

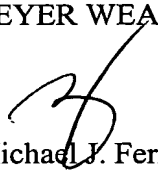
Therefore, in contrast to the cited references, the invention as recited in claim 11 describes a non-atomic "annotated assignment decision diagram" approach to logic simulation by use of control nodes annotating an associated assignment decision diagram. Therefore, the control nodes afford the ability to observe the states **within** a particular process block and not just the global (i.e., atomic) state of a process block as required by the cited references. Since none of the secondary references teach or even remotely suggest control nodes to view an internal state of a process block, the Applicant believes that claim 11 and its associated dependent claims 12 – 26 are allowable over the cited references taken singly or in any combination.

The Examiner rejected claims 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,848,236 issued to Dearth in view of U.S. Patent 5,937,190 issued to Gregory further in view of Chaiykul. Dearth simply teaches computer program product that specifies a method of compiling a simulation object used by a simulator to simulate the operation of a digital circuit and does not teach or even remotely suggest use of control nodes to provide a non atomic view of a state within a particular process block. Since none of the secondary references teach or even remotely suggest control nodes to view an internal state of a process block, the Applicant believes that claims 27 and 28 are allowable over the cited references taken singly or in any combination.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all pending claims are allowable. Should the Examiner believe that a further telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



Michael J. Ferrazano
Reg. No. 44,105

P.O. Box 778
Berkeley, CA 94704-0778
(650) 961-8300